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NANOPOROUS SILICON MEMBRANE FOR BIOMOLECULAR SEPARATION

H. V. BALACHANDRA ACHAR* and ENAKSHI BHATTACHARYA†
Microelectronics and MEMS Laboratory
Electrical Engineering Department
Indian Institute of Technology Madras
Chennai 600 036, India
**hvbachar@smail.iitm.ac.in*
†*enakshi@iitm.ac.in*

Separation of biomolecules based on their size and charge is an important procedure employed in biomolecular analysis. Nanosieve comprising of a semi-permeable membrane with nanometer-sized pores is used for this purpose. Described here is the fabrication of ultra thin nanoporous silicon membrane, which can be used as nanosieve, making use of standard microelectronics fabrication techniques. Lithography and bulk silicon etching is used to initially create a 10 μm thick sacrificial membrane in the center of a 200 μm thick silicon substrate. A three-layer stack of SiO_2, amorphous silicon (a-Si) and SiO_2 is then deposited using chemical vapor deposition technique. The sample is subjected to rapid thermal annealing during which pores are formed in the a-Si layer. Finally, the 15 nm thick nanoporous silicon membrane is released using reactive ion etching of the sacrificial membrane. The formation of the pores is confirmed by transmission and scanning electron microscope images. At present the pore formation is random; our future work will focus on controlled nucleation of silicon nanocrystals so as to get pores at desired locations.

Keywords: Nanopore; nanoporous silicon.

1. Introduction

Classification of biomolecules based on their size and charge is one of the scheduled practices in the field of biomolecular analysis.[1] Nanosieve is a device which can be used for this purpose. Currently the molecules are separated using porous gel structures by electrophoresis.[2] But they have the disadvantage that molecules take longer time to pass through the porous structure, and there is a high possibility of molecules clogging the pores. Silicon nanosieve is an attractive alternative for such applications. The primary advantage is that silicon semi-permeable membranes can be made as thin as their biological counterparts, so that the molecules can traverse quickly through the pores, without the fear of clogging.

Several methods are discussed in scientific literatures for fabricating nanoporous membranes which can be used as nanosieves. Anodic aluminum oxide membranes fabricated using electrochemical etching is probably the earliest and widely studied nanoporous membrane.[3] Researchers have succeeded in producing defect-free porous anodic alumina membranes with thickness in millimeters and pore diameter of the order of 100 nm. Electrochemical etching has also been used to fabricate nanoporous silicon and germanium membranes.[4]

However, recent trend in nanoporous membrane production has been to use the silicon fabrication techniques. Silicon and silicon nitride nanoporous membranes have been successfully fabricated using

lithography and focused ion beam (FIB) drilling, which have narrow pore size distribution, good mechanical strength and biochemical stability. Such membranes with pore size down to 25 nm and membrane thickness 1−5 μm have been successfully implanted in pancreas and used in drug delivery systems.[5] However, FIB requires sophisticated instruments and is an expensive process.

As an alternative to direct patterning of pores on semiconductor surface, Striemer *et al.*[6] discovered that when a thin layer of amorphous silicon (a-Si) sandwiched between two layers of SiO_2, is rapidly annealed at high temperatures for 30 s, spontaneous voids are formed in the material due to volume contraction and material strain. This technique has been used to form random pores on thin nanocrystalline silicon frame, having extremely high mechanical strength which can withstand differential pressure of 1 atm. The authors have successfully tested the passage of smaller proteins through the pores, while the larger ones got blocked.

Striemer *et al.*[6] used RF magnetron sputtering to deposit a-Si stacked between two layers of SiO_2, over polished crystalline silicon substrate. After rapid thermal annealing process, they etched the backside silicon substrate using EDP chemical etchant, so that nanoporous membrane is formed on the top surface.

Our aim is to form nanoporous membranes by Striemer's technique but using chemical vapor deposition (CVD) for depositing the a-Si layer instead of RF sputtering. Both low pressure CVD (LPCVD) and plasma enhanced CVD (PECVD) can be used. Since CVD allows a better control on deposition, we hope to control the nucleation of the pores on the silicon surface. We also wish to investigate the effect of the presence of hydrogen in the a-Si films in the pore formation. Our final goal is to explore the translocation of biomolecular particles through nanoporous silicon membrane in a microfluidic chamber filled with electrolyte, so as to precisely determine the size and charge of the particles. Towards this effect, experiments were done at the University of Bologna, Italy, with silicon nitride nanopore membranes sourced from AppNano, USA. Duration and magnitude of current dip when spherical charged particles traversed through the nanopore were successfully measured.[7]

Described in this paper is fabrication of ultra thin nanoporous silicon membrane using standard micro fabrication techniques. The fabrication steps detailed in the next section revolves more or less around the principle adopted by,[6] but instead of forming the membrane on the surface, we have fabricated it in the middle of the substrate cross section. As a result the membrane is sturdier and hence handling becomes easier.

2. Fabrication Steps

Samples are prepared from 200 μm thick double-side polished 100 mm diameter *p*-type ⟨100⟩ silicon wafer. The wafer is cleaned using standard silicon wafer cleaning procedures comprising of primary and RCA cleaning steps. A thick thermal oxide layer of thickness 0.8 μm is grown on both sides of the wafer at 1000°C (Fig. 1(a)). Windows of dimension 400 μm × 400 μm are first opened on the top side oxide layer, and then aligning the mask perfectly with the front side pattern, windows are opened in the bottom side oxide layer (Fig. 1(b)).

Using the patterned oxide as the mask, bulk silicon is etched simultaneously from both sides of the wafer in 44.4 wt.% KOH solution with nitrogen

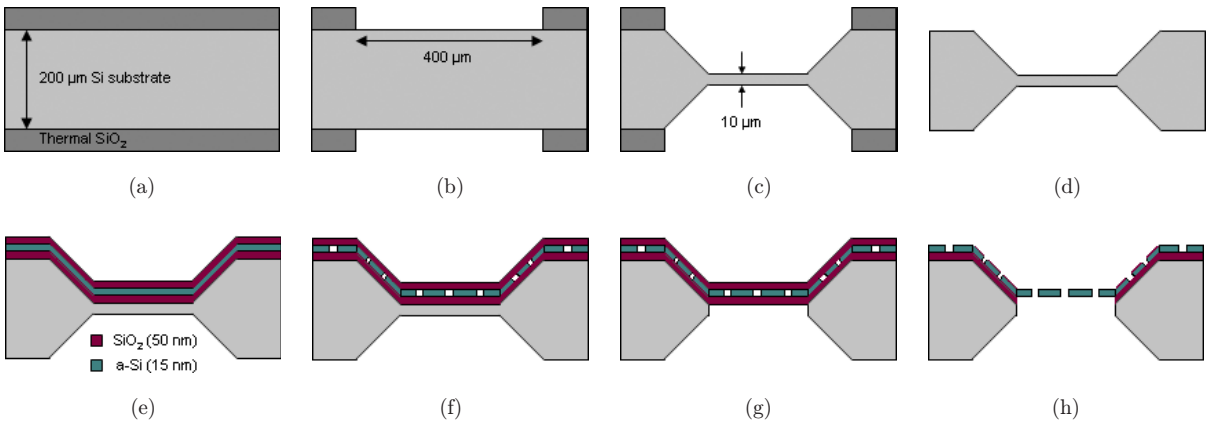

Fig. 1. Fabrication steps.

bubbling, maintained at a constant temperature of 80°C. Etching is carried out until a sacrificial membrane of thickness 10 μm is formed at the center of the wafer cross-section (Fig. 1(c)). The left over oxide is removed by dilute HF dip (Fig. 1(d)). RCA cleaning is again carried out to remove any K^+ ions on the wafer surface, which may contaminate the furnace during the next process step.

A three-layer stack of SiO_2, a-Si and SiO_2 of thicknesses 50 nm, 15 nm and 50 nm respectively, is deposited on the patterned wafer surface (Fig. 1(e)). PECVD technique is used for SiO_2 deposition, and LPCVD technique is used for a-Si deposition. We have previously optimized the deposition recipes for both PECVD and LPCVD to get slowest possible deposition rates. When PECVD was used for a-Si deposition, we got deposition rate of approximately 20 nm min^{-1}, which was too high to reproducibly get a layer of 15 nm thickness. So we switched to LPCVD for a-Si deposition in which we could get deposition rate as low as 0.75 nm min^{-1}.

The deposition condition used for PECVD SiO_2 deposition is: 300°C temperature, 200 m Torr chamber pressure, 10 W RF power, 6 sccm silane, 94 sccm nitrogen and 80 sccm nitrous oxide flow rate. Deposition condition for LPCVD a-Si deposition is: 550°C temperature, 250 m Torr pressure and 10 sccm silane flow rate.

The wafer, along with the as-deposited 3-layer stack is subjected to rapid thermal annealing (RTA) at a temperature of 750°C for 30 s in nitrogen ambient. During this phase, the amorphous silicon transforms itself into nanoporous silicon (np-Si), leaving voids in the material. The voids span the entire thickness of the layer forming pores (Fig. 1(f)). The diameter and density of the pores depend on the annealing temperature.

The 10 μm sacrificial Si membrane is now removed using reactive ion etching (RIE) until the bottom SiO_2 layer is reached (Fig. 1(g)). Finally both the top and bottom oxide stacking layers are stripped using buffered oxide etchant, leaving behind the free standing np-Si membrane (Fig. 1(h)). The entire fabrication process is outlined in Fig. 1.

3. Results and Conclusions

Plan-view transmission electron microscopy (TEM) image of np-Si membrane is shown in Fig. 2. The bright spots are nanopores, whereas the grey and black portions are nanocrystalline silicon. The diameter of the pores varies from 10 nm to 75 nm.

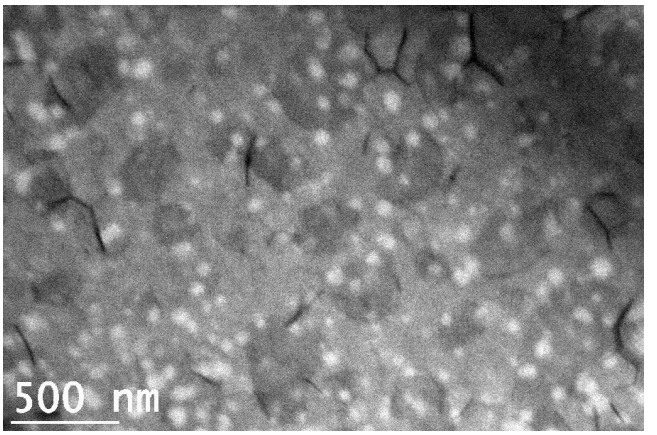

Fig. 2. Plan view TEM image of nanoporous silicon membrane.

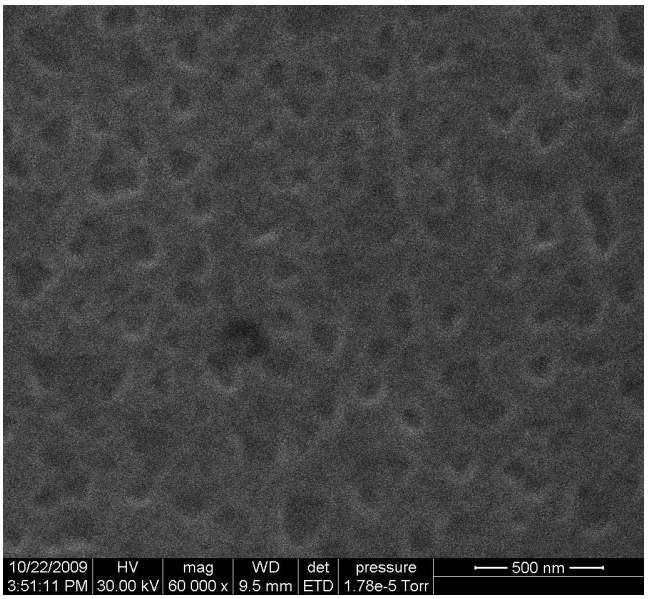

Fig. 3. SEM image of nanoporous silicon membrane.

Scanning electron microcopy (SEM) image of the membrane is shown in Fig. 3. The nanopores appear as dark spots in the image. It may be noted that different samples were used for obtaining TEM and SEM images.

An important factor that needs to be addressed is the tunability of pore size. In principle it is understood that pores are formed when a-Si is rapidly annealed above 700°C, and that the pore diameter increases with increase in annealing temperature.[8] This needs to be studied and experimented so as to fabricate pores of precise diameters.

Moreover, at present the pore formation is spontaneous and random in nature. Our future work will also focus on controlled nucleation of silicon nanocrystals so as to get pores at desired locations.[9]

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