

Glass-to-glass anodic bonding with standard IC technology thin films as intermediate layers

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Abstract

Glass-to-glass wafer bonding has recently attracted considerable interest. Especially for liquid manipulation applications and on-chip chemical analysis systems, all-glass sealed channels with integrated metal electrodes are very attractive. In this paper, we present a novel anodic bonding process in which the temperature does not exceed 400°C. This is a crucial requirement if metal patterns are present on the wafers. A number of thin film materials available in most conventional IC processes deposited on the glass wafers have been tested as intermediate bonding layers. Successful bonding is obtained for various layer combinations and an explanation of the bonding mechanism is given. © 2000 Elsevier Science S.A. All rights reserved.

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1. Introduction

Micromachined analysis systems containing a combination of a capillary electrophoresis channel and a liquid conductivity detector are very interesting for online monitoring of bioprocesses such as cell cultures. After the electrophoresis separation procedure, the concentration of ions is determined by the conductivity detector, all on one chip. Due to the high voltage applied on the liquid during the capillary electrophoresis separation [1], a completely electrically insulated channel has to be fabricated. Glass-to-glass bonding is a very suitable solution to this problem. However, the glass-to-glass processes published to date require either high temperatures [2], which would damage aluminium patterns, or spin on glass [3] as intermediate layer, which would fill recesses, disturbing the channel definition. In this paper, a new glass-to-glass bonding process, which meets the mentioned demands, is described.

As glass-to-glass bonding is only possible with an intermediate layer, we looked at the possibility to use thin

films of materials available in most conventional IC processes. These materials are well-characterized and can be accurately patterned. The intermediate films investigated in our glass-to-glass bonding process are amorphous silicon, polysilicon, silicon nitride, silicon carbide, and silicon oxide or a combination of two or three of them. Temperatures not exceeding 400°C and voltages of around 700 V have resulted in successful bonding of patterned glass-to-glass wafers. The process, due to its simplicity, low cost, and compatibility with conventional IC fabrication processes, has high potential for many applications. Particularly, new fluid manipulation devices can largely benefit from the low temperature and flexibility in material choice offered by the bonding process presented here.

2. Experiments

Since anodic bonding of glass-to-silicon with a silicon oxide or nitride intermediate layer is possible [4,5], the presence of silicon at the bonding interface is obviously not required. This suggests that glass-to-glass bonding can be obtained when using a proper material as intermediate layer. Without any intermediate layer, glass-to-glass can-

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not be bonded anodically. In fact, due to the sodium diffusion to the interface, the high electric field, essential for the bonding to occur, is not created. Consequently, no intimate contact between the wafers takes place and the bonding fails. In order to attain anodic bonding, a sodium diffusion barrier has to be created.

For the experiments reported here, we used Pyrex no. 7740 wafers with a diameter of 100 mm and a thickness of 500 μm . To attain anodic bonding, one or both wafers were provided with a thin film (see Fig. 1). Different materials have been tested: amorphous silicon, polysilicon, silicon nitride, silicon carbide, and silicon oxide. Some wafers were covered with two of these layers. Generally, 200-nm-thick layers were used, except for the amorphous silicon where also a very thin layer of 20 nm was tested. Two deposition techniques have been used to coat the glass wafer with the intermediate layer. Polysilicon and amorphous silicon layers have been deposited using low-pressure chemical vapor deposition (LPCVD). The process parameters used are given in Table 1. For the polysilicon layers, the deposition was followed by an annealing step at 600°C. This annealing temperature is a little above the softening point of the glass which can cause a slight bending of the wafer. The silicon nitride, silicon carbide, and oxide layers are deposited in a Novellus plasma-enhanced chemical vapor deposition (PECVD) reactor using the parameters reported in Table 2.

Before bonding, the samples were cleaned in fuming nitric acid (100%) for 10 min, rinsed in water for 5 min, and spun dry. The bonding set-up is shown in Fig. 1. A layer indicated as “layer no. 1” coats the top wafer, while the bottom wafer is coated with “layer no. 2”. As explained in Section 3, the layer coating the bottom glass wafer (layer no. 2) can also be a combination of two layers.

Most of the experiments have been carried out at 400°C and 700 V. Generally, a bonding time of 10 min is sufficient for the bonding. However, for the combination of silicon nitride and oxide on the bottom wafer and oxide on the top wafer, 1000 V and 30 min were necessary. This is probably due to the increased total thickness of the insulating layer that results in a lower electric field at the bonding interface. Lower temperatures and voltages have

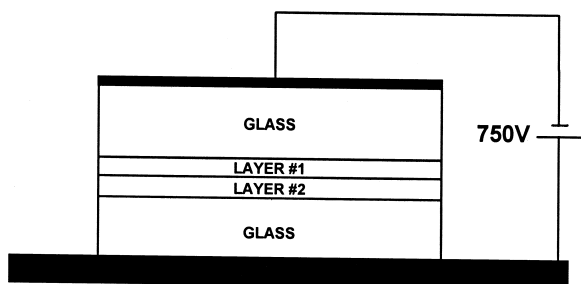


Fig. 1. Anodic bonding set-up.

Table 1
LPCVD deposition parameters

Layer	Gas flow (sccm)	Pressure (mTorr)	Temperature (°C)	Deposition rate ($\text{\AA}/\text{min}$)
Polysilicon	$\text{SiH}_4 = 45$	150	545 + 600	12
Amorphous silicon	$\text{SiH}_4 = 45$	150	545	12

been experimented as well and a high-quality bonding is obtained for many of the other combinations presented here.

3. Results

Wafers, provided with various combinations of intermediate films, have been anodically bonded. The results are shown in Table 3. A striking outcome is the fact that the intermediate layer on the Pyrex does not necessarily have to be electrically conductive. For glass-to-silicon anodic bonding, the silicon wafer has the function of the anode. During the glass-to-glass anodic bonding, the transport of charge takes place through both (heated) Pyrex wafers. Another remarkable result is that dramatically different bonding results can be obtained by exchanging layer nos. 1 (top wafer) and 2 (bottom wafer). In fact, oxide as layer no. 2 never results in a bonding (see Table 3, row 4), except when another layer is present underneath. On the other hand, oxide as layer no. 1 gives a good bonding with nitride and silicon (column d). This can be explained by considering that layer no. 2 has the function of a diffusion barrier for sodium ions which migrate towards the cathode. This barrier prevents them from reaching the surface and a high electric field over the intermediate area will be generated. This high field leads to a strong attraction of both wafers and subsequent bonding between them. However, no bonding will occur if the sodium ions are present directly at the bonding interface. This is the case when layer no. 2 is formed by oxide, a material that does not function as a diffusion barrier. The double layer experiments confirm our explanation. Oxide as layer no. 2 could never result in a successful bonding (row 4). However, when a nitride or silicon film was placed between the Pyrex and the oxide, a successful bonding resulted with a non-covered or oxide-covered Pyrex wafer (rows 7 and 8) as sodium ions migration is now impeded. When layer no. 1 consists of silicon (either poly or amorphous) or nitride, no bonding will occur (columns b, c, and e), probably due to the lack of oxygen ions at the interface.

In order to verify the proposed bonding mechanism, transmission electron microscopy (TEM) and energy dispersive X-ray spectroscopy (EDS) measurements were made on a sample with oxide as layer no. 1 and nitride as layer no. 2. The results are shown in Figs. 2 and 3.

Table 2
PECVD deposition parameters

Layer	Gas flow (sccm)	HF power (W)	LF power (W)	Pressure (Torr)	Temperature (°C)	Deposition rate (Å/min)
Silicon nitride	N ₂ = 1000 SiH ₄ = 280 NH ₃ = 1800	320	480	2.8	400	1820
Silicon carbide	SiH ₄ = 100 CH ₄ = 3000	500	500	2.25	400	700
Silicon dioxide	N ₂ = 3150 SiH ₄ = 205 N ₂ O = 6000	1000	0	2.2	400	4380

Table 3
Glass-to-glass bonding results for different intermediate layers (+, strong bonding; -, no strong bonding obtained)

Layer no. 2	Layer no. 1					
	(a) None	(b) Polysilicon	(c) Nitride	(d) Oxide	(e) α-Silicon	(f) Carbide
(1) None	-	-	-	-	-	-
(2) Polysilicon	+	-	-	+	-	-
(3) Nitride	+	-	-	+	-	-
(4) Oxide	-	-	-	-	-	-
(5) α - Silicon	+	-	-	+	-	-
(6) α - Silicon/nitride	+	-	-	+	-	-
(7) Carbide	+	-	-	+	-	-
(8) Nitride/oxide	+	-	-	+	-	-
(9) α - Silicon/oxide	+	-	-	+	-	-

The high sodium concentration in the nitride is an indication that sodium diffuses in the nitride much slower than in the oxide. It means that if the oxygen from the top wafer reaches the interface earlier than the sodium of the bottom wafer, which seems to be the case for that sample, the oxygen can react at the interface, which results in a strong bonding.

The samples show a bond strength, which is too strong to measure by the crack opening method [6]. It is impossible to insert the blade at the bonding interface.

The oxygen concentration at the interface shows that the oxygen diffuses during the bonding process into the nitride oxidizing the top layer of the nitride. A thin oxide layer of about 10 nm in thickness is grown during the bonding. The TEM picture (Fig. 3) is supporting this theory, too. The bonding and the oxide–nitride interfaces are not identical. Some gas is trapped at the bonding interface during bonding as indicated by the light areas on

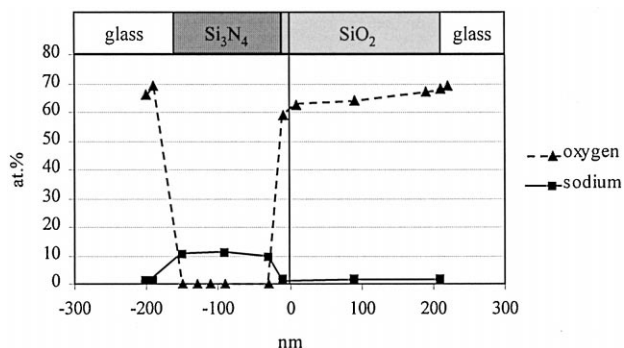


Fig. 2. EDS results of the specimen.

the picture due to the surface roughness of the PECVD layers. It is clearly visible that the oxide is grown into the nitride layer. The total thickness of the nitride layer is (after bonding) less than the original thickness. The PECVD nitride layer is deposited in seven steps, which can be recognized in Fig. 3 as seven layers with the same thickness. Only the layer at the interface is evidently thinner and the bond interface would correspond to the thickness

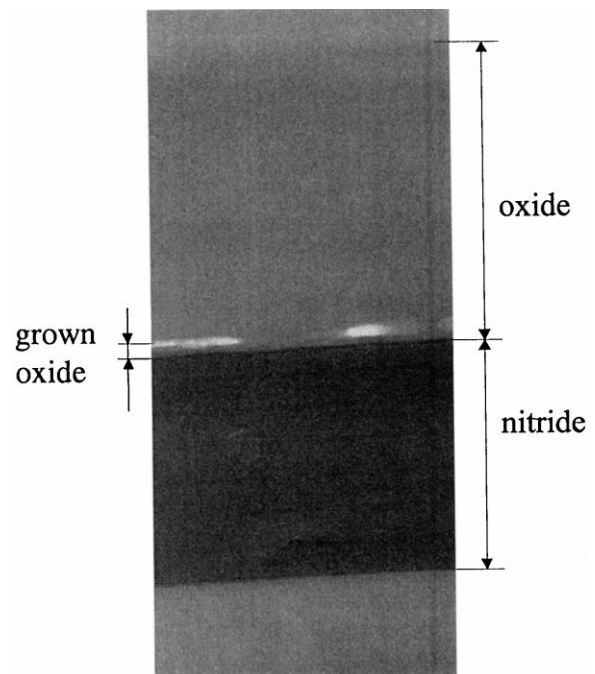


Fig. 3. TEM picture of the specimen.

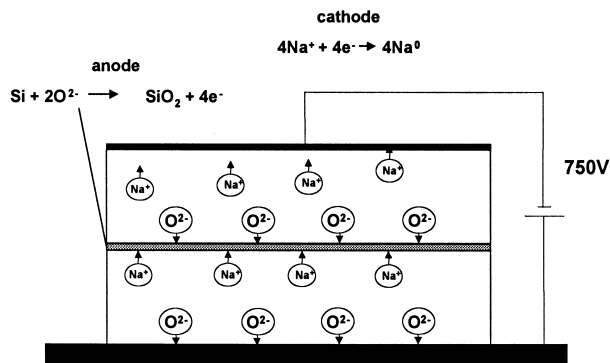


Fig 4. Glass-to-glass bonding mechanism.

of the other layers. Since the nitride has a thickness of about 160 nm, the grown oxide can be estimated at 8–10 nm.

4. Bonding mechanism

Our results can all be explained if we look into the bonding mechanism.

Before bonding, the wafer stack is heated up to 400°C. At elevated temperatures, the sodium oxide splits up in sodium and oxygen ions. When the electric field is applied during anodic bonding, these ions move. The transport of charges takes place through both Pyrex wafers (Fig. 4). Sodium is migrating towards the cathode and will be neutralized there. In the wafer on the anode, the migration of sodium ions is decreased in the deposited layer, which, in the case of silicon, silicon nitride and silicon carbide, is a diffusion barrier. Due to the high electric field, the wafers are attracted and the oxygen ions are moving towards the anode and react at the interface with the silicon of the bottom wafer forming an irreversible silicon–oxygen–silicon bond between both wafers.

5. Conclusions

A novel glass-to-glass bonding process, in which the temperature does not exceed 400°C, has been developed. Several thin film materials have been used as intermediate layer. Successful bonding is obtained when the wafer on the anode is coated with any of the material investigated, except oxide. If oxide is present or required, an additional polysilicon or nitride layer is added to obtain the bonding. The bond strength of the combinations is very high. It is impossible to separate the wafers at the bond interface. This low-temperature bonding process, due to its simplicity, low cost, and compatibility with conventional IC fabri-

cation processes, has high potential for many applications. Particularly, new fluid manipulation devices, e.g., CE devices and chemical microreactors, can largely benefit from the low temperature and flexibility in material choice offered by the bonding process presented here.

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Biographies

Axel Berthold was born in 1968 in Borna, Germany. In 1991, he started studying Electronics at the TU Chemnitz-Zwickau. In 1995, he came to the Delft University of Technology under the Erasmus Student Exchange Program to work in the field of IC-compatible silicon fusion bonding. In 1996, he received the MSc degree in Electrical Engineering from the TU Chemnitz-Zwickau. Currently, he is a PhD student at the DIMES Research School of the Delft University of Technology on the topic of new technologies for physical chemosensors.

Michael J. Vellekoop was born in 1960 in Amsterdam. He received the BSc degree in Physics in 1982 and the PhD degree in Electrical Engineering in 1994. From its foundation in 1988 until 1995, he was managing director of Xensor Integration. Currently, he leads the physical chemosensor group at the Electronic Instrumentation Laboratory of DIMES, Delft University of Technology.

Lucia I. Nicola was born in 1973 in Bolzano, Italy. In 1992, she started studying Materials Engineering at the Università degli studi di Trento. In 1998, she came to the Delft University of Technology under the Erasmus Student Exchange Program to work in the field of glass-to-glass anodic bonding. In 1999, she received the MSc degree in Materials Engineering from the Università degli studi di Trento. Currently, she is a PhD student at the Delft University of Technology.

Pasqualina M. Sarro (IEEE Member 1984; Senior Member 1997) received the Laurea degree in Solid States Physics from the University of Naples, Italy, in 1980. From 1981 to 1983, she was a post-doctoral fellow in the Photovoltaic Research Group of the Division of Engineering, Brown University, Rhode Island, USA, where she worked on thin film photovoltaic cell fabrication by chemical spray pyrolysis. In 1987, she received the PhD degree in Electrical Engineering at the Delft University of Technology, the Netherlands, her thesis dealing with infrared sensors based on integrated silicon thermopiles. Since then, she has been with the Delft Institute of Microelectronics and Submicron Technology (DIMES), at the Delft University, where she is responsible for research on integrated silicon sensors and microsystems technology. Since April 1996, she has been serving as Associate Professor in the Electronic Components, Materials and Technology Laboratory of the Delft University. She has served as technical program committee member of the ESSDERC Conferences (since 1995), the SPIE 5th Annual Symposium on Smart Structures and Material '98 and Eurosensors '99.